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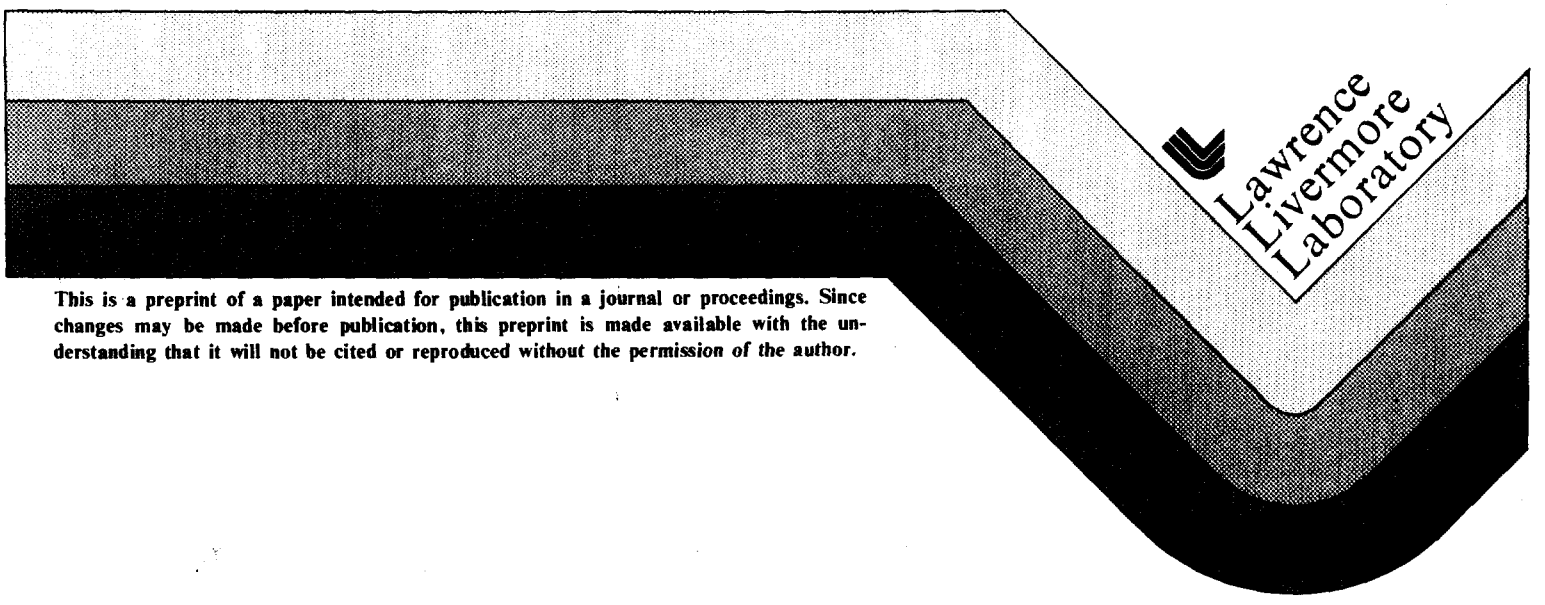

CAMAC SERIAL HIGHWAY INTERFACE FOR THE LSI-11

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ABSTRACT

A CAMAC Serial Highway Interface has been designed for the Local Control and Instrumentation System of the Mirror Fusion Test Facility. There are over 50 distinguishable systems in the facility, each of which consists of the LSI-11 computer, fiber optic communication links, and the CAMAC system. The LSI-11 computer includes a 32k memory, serial modem interface and the CAMAC Serial Highway Interface.

The Serial Highway interface uses the DEC Q-Bus protocol chips for program control and DMA interface to the LSI-11. It converts the Q-bus oriented data to the standard CAMAC Serial Highway message format and vice versa. Transverse and vertical message parity generation and checking are performed. Message synchronism is automatically sent to the Serial Crate Controller, and any data transmission errors will be reported to the computer. It separates demand messages from regular reply messages and stores them in the First-In-First-Out buffer.

The Serial Highway Interface includes a Block Transfer function which allows large block of data in the CAMAC system to be transferred to the computer memory though the DMA port of the LSI-11 computer.

INTRODUCTION

The Lawrence Livermore Laboratory Mirror Fusion Test Facility (MFTF) is a large magnetic confinement system. Operation of MFTF will provide the means to answer many of the plasma physics and engineering questions. The successful MFTF will be a significant step closer to operational, power producing fusion reactors by the end of this century.

The MFTF consists of many major engineering systems such as:

- Superconducting Magnet System
- Neutral Beam Injectors
- Confinement Vessel System
- External Vacuum System
- Cryogenic System
- Electrical Power System
- Control and Diagnostic System

The complexity of MFTF requires a decentralized multi-level control system. The beam injectors exemplify this complexity. There are 24 sustaining neutral beam injectors, each of which consists of five different types of power supplies; 20 start-up neutral beam injectors, each of which has four different types of power supplies; and 60 plasma streaming guns, each assembly of which is associated with a gun and a magnet power supply. All these power supplies have to be monitored and controlled individually. Other systems including hundreds of sensors, thousands of safety interlocks, and a wide variety of diagnostic instruments have to be recorded.

The MFTF control and diagnostics system is handled by a distributed computer network consisting of 9 Interdata computer systems and more than 50 LSI-11 computers. The LSI-11 computers, which fall into the area of the Local Control and Instrumentation System (LCIS), are used to transfer local control information between the system and the Interdata computer systems of the Supervisory Controls and Diagnostic System (SCDS).

SYSTEM DESCRIPTION

During the course of the preliminary design of the LCIS, it became clear that as much as possible common hardware should be used in the controls for over 50 systems of MFTF for reasons of economics, ease of maintenance, reduction of design effort, and timely completion of the LCIS installation. This common hardware or "foundation system" shown in Figure 1 consists of three major subsystems, the local computer system, the fiber optic communication links, and the CAMAC system.

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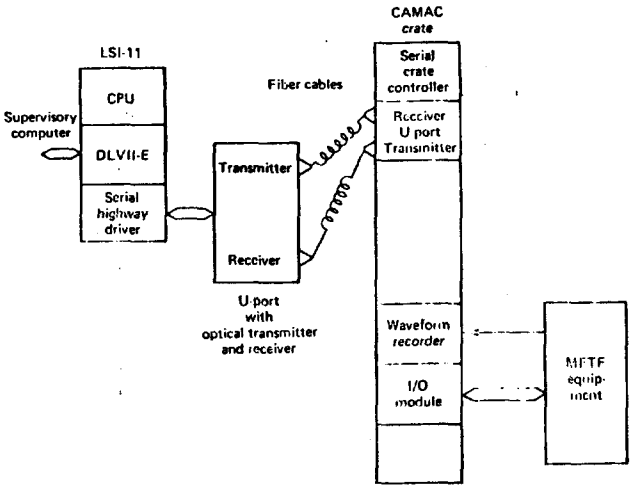

Figure 1 LCIS Foundation System

The local computer system includes an LSI-11 computer CPU, 32K word memory, a serial line modem interface, and a serial highway interface (SHI). The serial line modem interface is the DLV-11-E. It is used as an asynchronous serial line to communicate with the SCDS computer. The SHI establishes a Serial Highway (SH) for the Serial CAMAC. All terms associated with Serial CAMAC are described in Ref. 1.

The communication links between the LSI-11 computer and the remote CAMAC crate will be implemented with fiber optic links. The fiber optic links are duplex links of optical transmitters, receivers, and fiber cables. These optical transmitters and receivers can carry information at maximum data rate of 10 M b/s (Bi-phase or Manchester) over distances of up to 1 kilometer with a bit error rate of less than 10^{-9} at the maximum data rate.

The CAMAC system is the last major subsystem of the LCIS. Modules that are common to all systems include the Serial Crate Controller (SCC) and the U-port module of optical transmitters and receivers. The actual interface to the MFTF equipment being controlled is provided by a set of CAMAC compatible modules, either commercially available or designed in-house.

To make a CAMAC based LCIS economically feasible, a replacement for the standard method of implementing the SH with the LSI-11 computer was needed. The standard method represents the high cost of an LSI-11 Parallel Highway Interface, CAMAC crate and power supply, and serial highway driver. The decision to design a custom interface was based on the lack of a suitable commercially available interface.

SHI Design Overview

The design of the SHI for implementing the SH with the LSI-11 computer has been based on the application of the LCIS for MFTF. The requirements of the design are to provide:

- Program transfer;
- Block transfer with DMA reading;
- Both D-ports and U-ports of Bi-phase modulation;
- Bit-serial transmission of data rate 2-1/2 M b/s and 5 M b/s;
- Extended memory address lines for the LSI-11/23;
- Terminations for the Q-bus.

The SHI design is packaged in a double size and a quad size module directly plugged into the computer backplane. The double size module, the Transmitter, consists of four 16-bit word or eight 8-bit byte write-only registers, which convert the LSI-11 data into the SH Command message format. There are two counters, the bit-frame counter of 12-bit cycles and the message counter which has a 10-bit cycle for a Write command and a 6-bit cycle for a Read command. Transverse and vertical parities are generated during the loading of the byte registers into the 10-bit shift register. A selection of transmission rate has to be made before installation. The one bit control register, when set, will initiate the bit-serial transfer through the D-ports and the U-port. The U-port transmits Bi-phase (Mark) signals where the clock and bit-data are modulated. It is intended to be used with an optical link.

The quad size module is the Receiver which provides D-port and U-port inputs. The Bi-phase signal from the U-port is decoded into NRZ data and clock just as those from the D-ports. The demodulated circuit uses a monostable multivibrator (one-shot) to regenerate the clock where 2.5 or 5 M b/s of transmission rate has to be set before the installation of the system. The Receiver module normally accepts input signals from the U-port which is intended to be used with the optical link. Selection of inputs from the D-ports automatically disables the U-port input.

The Receiver module accepts Wait bytes, Reply, and Demand messages. The Wait byte provides synchronization of the module. The transverse parity of every frame and the vertical parity of every message are checked. Any parity error detected and errors coming from the SCC are stored in the Status register and at the same time an interrupt is sent to the computer. The Receiver separates the Demand messages from the Reply messages and stores them in the 64 depth First-In-First-Out (FIFO) buffer. The presence of data in the FIFO will cause an interrupt of higher level to the computer for immediate attention. The Reply message is stored in the Select registers and a flag is raised in the Status register for program transfer, or a service request to the DMA control is made when Block Transfer Mode (BTM) is selected. The loading of the word count and the bus address for DMA transfer are set up in the Receiver module. The BTM is terminated by a no Q-response from the addressed CAMAC module, word count zero, or any

error. The Receiver provides spaces for terminations of the Q-bus.

The Transmitter and the Receiver modules can be operated and addressed independently. There is only one signal across the two modules. This signal is needed when the BTM is selected.

The Transmitter Module

The Transmitter module, as shown in the block diagram of Figure 2, is interfaced to the Q-bus of the LSI-11 computer with five LSI chips manufactured by DEC. Four of the DEC chips are DC005 Transceivers which provide data and address information. The fifth chip is the DC004 Select Protocol logic which serves as a register selector of providing the signals to control data flow into four 16-bit word registers or eight 8-bit byte registers which are arranged in the order of Command messages as shown in Table 1. The functions of the DEC chip kit are described in Ref. 2. The output device select line (Sel) 0 writes from the D-bus into the Header byte register in which the Crate Address (SC) field indicates the destination of the message and Byte 2 register which contains the Subaddress (SA). Sel 2 writes into Byte 3 and Byte 4 registers consisting of the Function (SF) and Station Number (SN) of the Command. Sel 4 and Sel 6 (lower half word only) write into the next four registers Byte 5 to 8, containing the 24-bit write data which are omitted when the Command is a Read function. It should be noted that three LSI-11 half words of 24-bit data are converted into four bytes of data of the Serial CAMAC format. The most significant data bit of the Sel 6 will set the "Go" bit of the Control Register (CR), which initiates the output of the Command message from the Transmitter module.

As soon as the computer power is up, the Transmitter module is sending Wait bytes to establish synchronization and to provide a system clock to the SCC. The Transmitter generates a 10-bit frame in which the first bit is the Start bit, a logical "0". The next eight bits are the data bits of the byte. The last bit is a Stop bit which is always logic "1". Each byte frame is separated by two pause bits. Thus, each frame consists of 12 bits.

A 10 MHz crystal clock is used to provide a system clock rate 2-1/2 or 5 MHz in the SH. If other system clock rates are desired, a crystal clock of double that frequency must be used. The clock is divided by two or four depending on the selection of the data transmission rate, to obtain a split phase clock. One phase of the clock is used for shifting data and the other is used for bit counting. The bit frame counter has a cycle of 12 counts representing a 12-bit frame. The first count loads the data from the C-bus and the transverse parity bit into the shift register. The C-bus is an 8 bit tri-state bus output from the Command message byte registers. The first count also loads the data into the register of the vertical parity generator which provides the column-parity component of the Geometric Error-Detection. The second to tenth count shift the data into the SH. The end of tenth count shuts off the shift register. The 11th and 12th count provide pause bits. Each cycle of 12-counts will increment the message counter if it is enable.

When the "Go" bit in the CR is set, the message counter is enabled and will be incremented by one at the end of the data frame, thus, terminating the Wait bytes in the SH. Then the Command message will be output. If the Command is a Write function, a Sum byte from the vertical parity generator will be released at the ninth count of the message counter after sending the Crate Address, Subaddress, Function, Station Number, and four bytes of 24 bit data. The Sum byte will be released at the fifth count in the message counter if the Command is a Read function. The Sum byte is the last byte in that portion of the Command message carrying information to a SCC.

The Transmitter generates a fixed number (8) of Space bytes and then terminates the transaction by sending the End byte. It then continues to send Wait bytes until the "Go" bit is set again. In this mode of operation, there are few excess Space bytes, and thus, allow the opportunity for Demand message generation upstream from the addressed SCC. The last Space byte resets the "Go" bit and the message counter.

The Transmitter does not have the provision of stopping to generate the next Command message before receiving the reply to the previous one. As long as the "Go" register is reset, a new Command message will be accepted and executed. This allows two modes of operation. The software will have the option of not sending out another command until a reply from the previous command has been received, or a series of commands may be sent within a time limit and all the replies read as soon as possible. The latter operation assumes that the software will have sufficient time and speed to catch all the replies. There is no storage in the Receiver module to store all the reply data.

The Transmitter provides two types of outputs, the D-port outputs consisting of NRZ data and clock and the modulated Bi-phase output where the NRZ data and clock are encoded. Both types of outputs are balanced drivers to conform with EIA RS 422.

The "Go" bit can be set externally by a signal coming from the Receiver module. This signal will be active at the end of a DMA cycle when the BTM is selected.

THE RECEIVER MODULE

The interface logic to the Q-bus of the LSI-11 computer is contained in the DEC chips which are DC003, DC004, DC005, DC006, and DC010 as described in Ref. 2. Figure 3 shows the block diagram of the Receiver module. Four DC005's are used as Transceivers providing data, address, and vector information. The DC004 is the Select Protocol controlling data into and out of the read-write registers. The Interrupt Control of DC003 performs interrupt transactions in the computer that uses a daisy-chain type of arbitration scheme. It provides two interrupt channels labeled A and B with the A channel at a higher priority than B. Two DC006's are used to

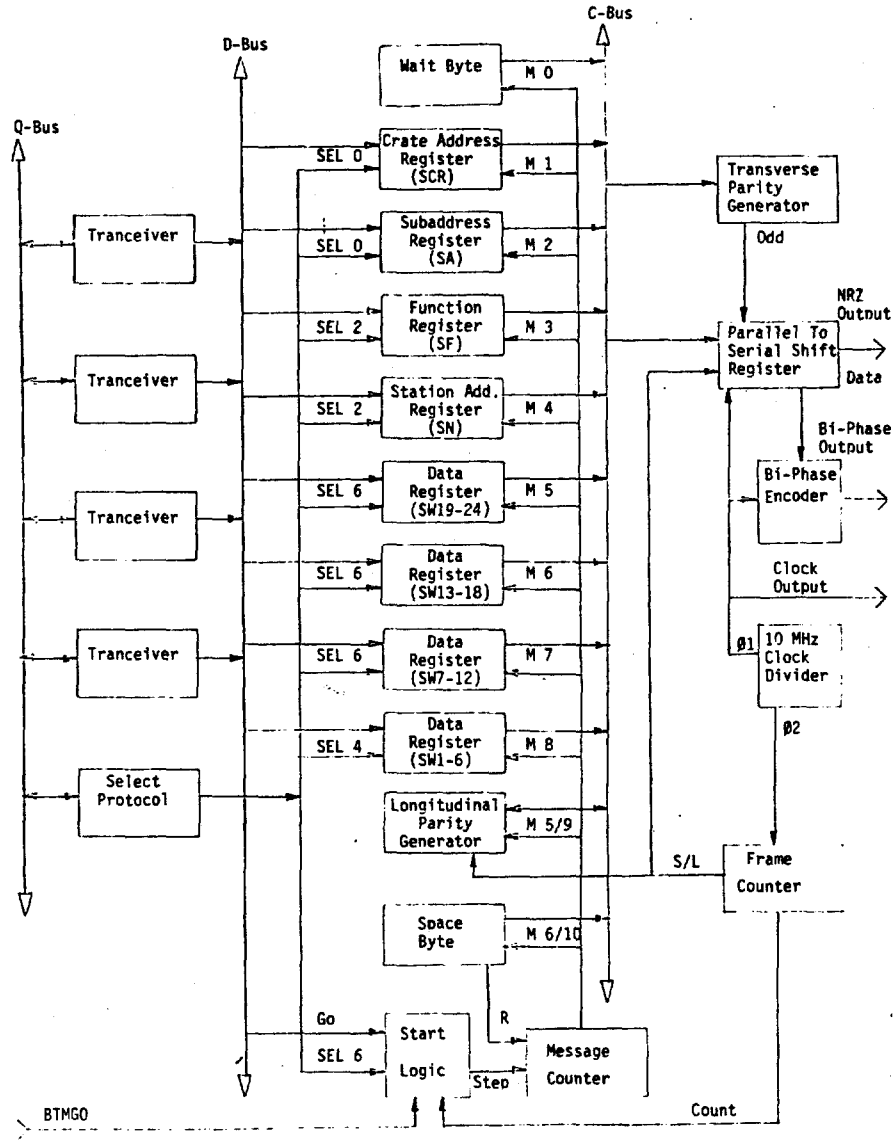

Figure 2 Block Diagram of the Transmitter

form a 16-bit word count and bus address counters for DMA transaction. These counters can be read, written, and incremented. The DC010 provides DMA control and timing logic to perform the hand-shaking operations required to request and gain control of the bus.

In the DC004 chip the output Sel 0 and Sel 2 write a 16 bit bus address and word count respectively into the counters of the DC006's for DMA operation from the tri-state DIO-bus. Output Sel 6 sets flags in the Control Status Register (CSR) of the Receiver module. Bit 8 and 9 of the CSR enables interrupt channel A and B of the DC003. Bit 10 clears the FIFO buffer and Bit 11 selects BTM during which all data read are transferred to the computer memory through the DMA port of the LSI-11 computer. The LSI-11/23 computer uses extended memory address lines 16 and 17. For BTM operation, if data read are to be stored in the extended memory area of the LSI-11/23 computer, bits 13 and 14 will accomplish this purpose. Sel 4 can only select read register and allows the Demand message into the DIO-bus. All Demand messages are stored in the FIFO. When the 1st Demand message arrives at the output of the FIFO, interrupt channel A in the Interrupt Control is triggered. The software should read all the Demand messages in the FIFO until the FIFO is empty. Bit 15 of the Sel 4 read register indicates this. When the BTM is selected, input Sel 0 and Sel 2 read the bus address and word count respectively from the DC006's. When the BTM is not selected, Sel 0 reads the Header byte and Byte 2 of the Reply message. Sel 2 and Sel 6 read the 24-bit data returning from the SCC. The upper byte of input Sel 6 reads the Status register. The bit assignments of the Status registers are:

Bit 15 - Data ready, indicating the presence of the Reply message.

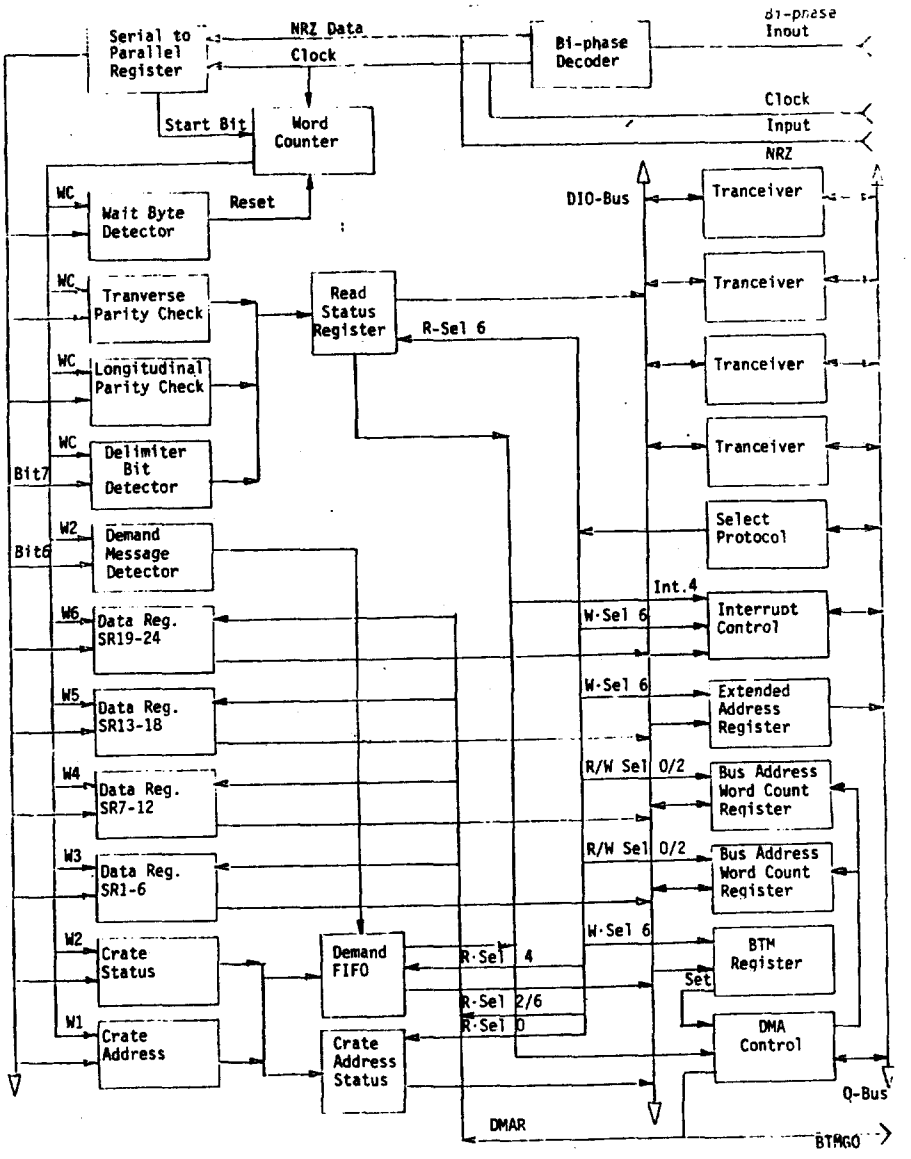

Figure 3 Block Diagram of the Receiver

Bit 14 - DMA time-out, indicating non-existent address, thus, terminating BTM operation.
Bit 13 - Word count zero, specifying successful completion of BTM.
Bit 12 - Line broken, indicating that the communication link between the CAMAC crate and the SHI is broken.
Bit 11 - BTM selected.
Bit 10 - Transmit error, including no x-response, no Q-response when BTM is set, ERR, and DERR.
Bit 9 - Transverse parity error detected.
Bit 8 - Vertical parity error detected.

Figure 4 shows all the SHI select registers.

Interrupt channel B will be triggered if any flags in the Status register except Bit 11 and 15 are set. In Program transfer, the software is required to scan the Data-ready bit in the Status register after a Command message has been issued. The Reply message will only be valid if the Data-Ready bit is present and no errors occur.

The Receiver module accepts D-port inputs and U-port input of modulated Bi-phase, both of which are designed to meet the EIA RS422 requirements. The Bi-phase input is decoded into NRZ data and clock, just as the D-port inputs. The NRZ data is shifted into a 10 bit Serial to Parallel register at the trailing edge of the clock. The Start bit of the serial frame, when it reaches the last stage of the shift register, will inhibit any shift function. The 11th bit-clock is used to find out if the incoming frame is a Wait byte or not. If it is a Wait byte, it will reset the Word counter and the Shift register. If it is not a Wait byte, it will enable the Word counter and will increment the Word counter by one at the rising edge of the 12th clock bit. It then strobes the data into the Reply message registers at the tailing edge and then resets the shift register. There are six 8-bit registers for the Reply message, and they are arranged in

the order of the Reply and Demand messages returning from the SCC, as shown in Table 2.

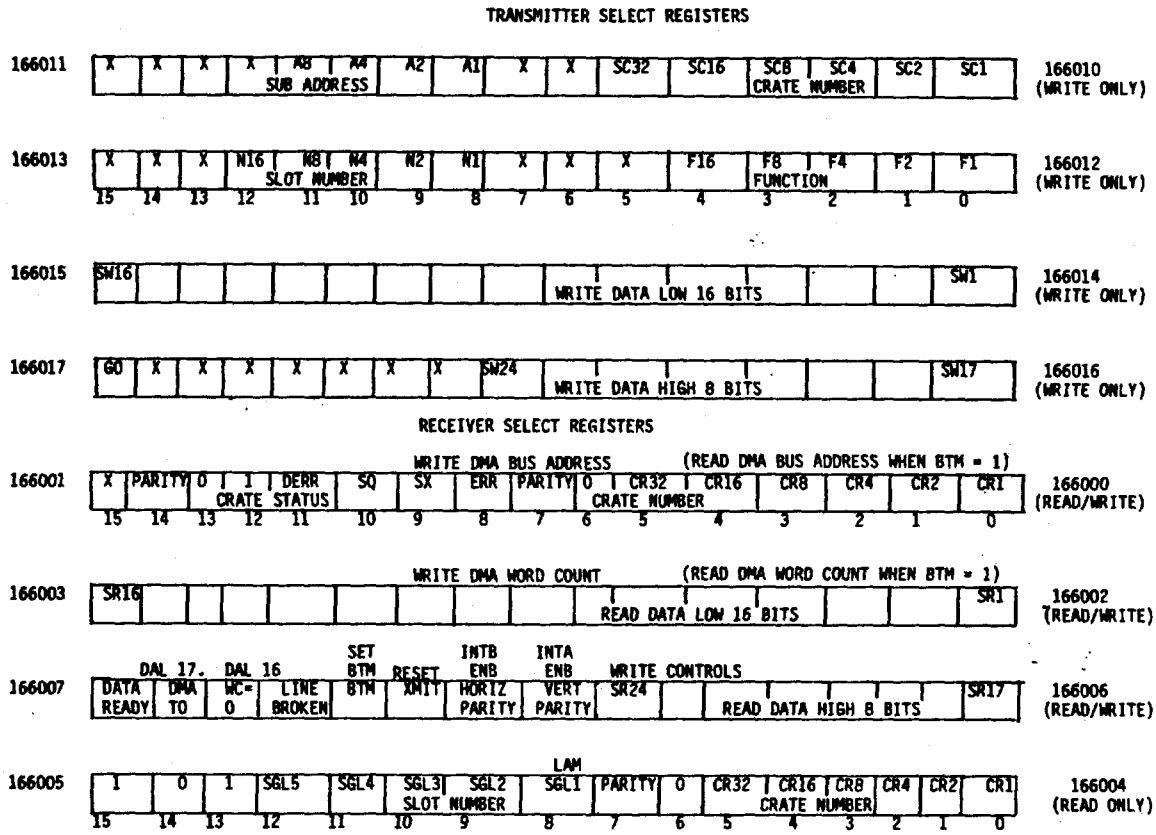

Figure 4 SHI Registers

The first incoming data frame after the Wait byte is stored in the Crate address register. As the Word counter is incremented, the next frame will be stored in the Crate Status register, and then maybe the next four data registers, depending if the Reply message is for a Read or Write Command message. The Write-Reply and Demand messages are three-byte messages while the Read-Reply message consists of seven bytes. In both cases, only the Endsum byte has the Delimiter bit set, which indicates termination of the Reply or Demand messages. The Receiver is constantly checking if the message Identifier M2 of every incoming message is set or not. If it is set at the second byte, the Delimiter bit of that message will automatically store that Crate address of the Header byte and the SGL field of the second byte into the Demand FIFO. If M2 is not set, the Delimiter bit of that message will raise the Data ready flag in the Status register, and stores the Crate address of the Header byte and the Crate status of the second byte into a select register, thus allowing it to be read by the computer.

If the BTM is selected, the Data Ready will raise a service request to the DMA control chip DC010. The DC010 performs handshaking operations required to request and gain control of the LSI-11 bus for DMA non-processor request data transfers. At the end of a single word transfer, a signal is sent to set the "Go" bit in the CR of the Transmitter module and the cycle of sending the Command message is repeated until the BTM is terminated by a successful end of word count zero or an unusual end of any detected errors. Only 16-bits of data are read into the memory of the computer.

Every frame of a message is checked for transverse parity. If the parity error is detected, a flag will be raised in the Status register and interrupt channel B will be triggered. This error flag indicates that there is one or more transverse parity errors in the incoming message. To locate where the error occurs needs some programming effort. The parity bits in the Header byte and the second byte are included in the Read register or Demand FIFO. All parity bits in the reply data and the End-sum byte are omitted.

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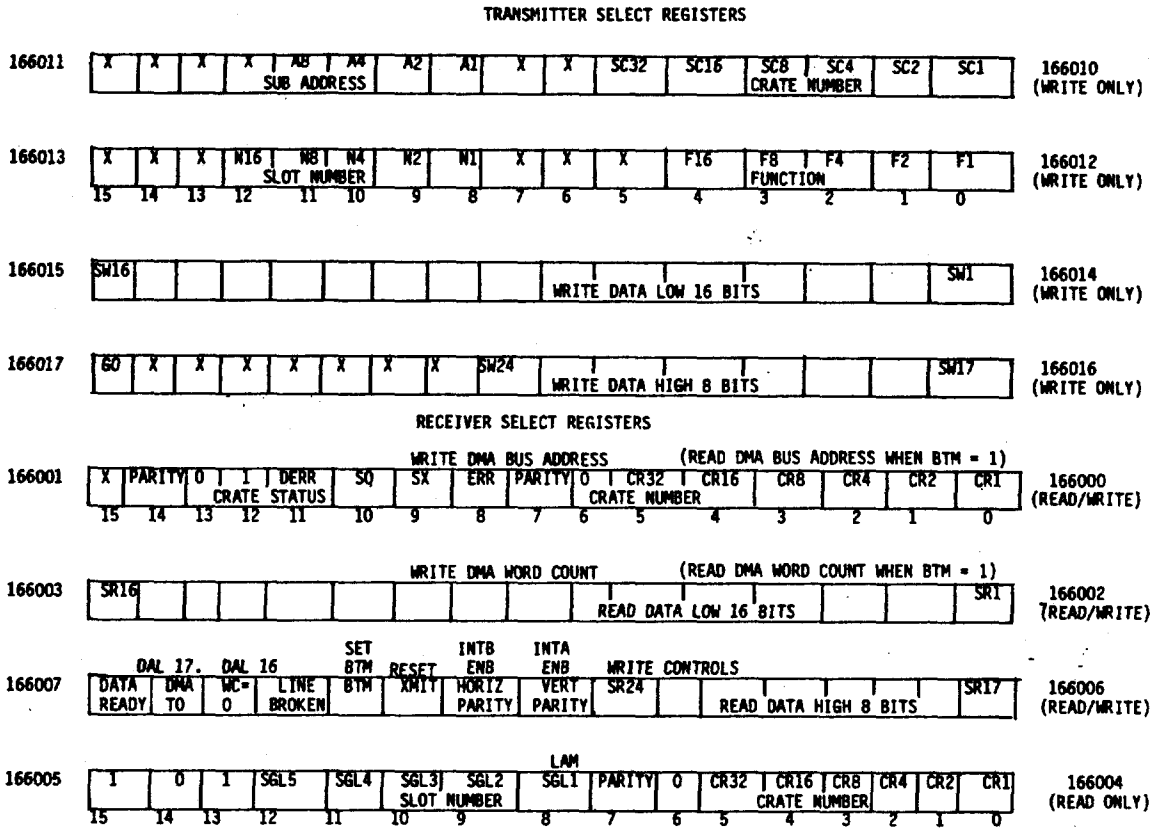

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The Receiver module generates the vertical parity of all Reply messages, and checks against the one generated by the addressed SCC. If such an error is detected, a flag will be raised in the Status register.

The Receiver module has been designed to receive Reply and Demand messages. It will ignore truncated Command messages and the Command messages for non-existant crates in the SH. Since there is no column-parity field in the truncated Command message, and no Delimiter bit in the End byte of the Command message, therefore, the Receiver module simply ignores these types of messages. The hardware could have a time-out feature to flag these messages. But a signal wire is needed across the two modules. In order to minimize the number of wires across the boards, it has been decided that the software should have its own time-out for every Command message.

CONCLUSION

The SHI design offers a simple and economical solution for providing a SH in the "foundation system" of the LCIS. At the time of writing this paper, production of the final P.C. boards is being made. However, there are several Serial CAMAC systems using early versions of the SHI P.C. boards, setting up for software development, module design development and long term reliability tests.

ACKNOWLEDGEMENTS

I want to express my appreciation to W. Labiak for his valuable suggestions and his contribution of software; to D. Peterson for his efforts in the construction and testing of the prototype.

REFERENCES

1. CAMAC Instrumentation and Interface Standards: Serial Highway Interface System (CAMAC), ANSI/IEEE Std. 595-1976, Published by the IEEE, Inc.

2. Chipkit Users Manual by Digital Equipment Corporation.

MSB 8	7	6	5	4	3	2	LSB 1	
b	0	SC32	.	.	.	.	.SC1	HEADER BYTE
b	0	0	. 0	.SA8	.	.	.SA1	BYTE 2
b	0	1**	.SF16	.	.	.	.SF1	BYTE 3
b	0	1**	.SN16	.	.	.	.SN1	BYTE 4
b	0	SW24	.	.	.	.	.SW19	BYTE 5 *
b	0	SW18	.	.	.	.	.SW13	BYTE 6 *
b	0	SW12	.	.	.	.	.SW7	BYTE 7 *
b	0	SW6	.	.	.	.	.SW1	BYTE 8 *
b	0	c	. c	. c	. c	. c	. c	SUM BYTE
1	0	1	. 1	. 1	. 1	. 1	. 1	SPACE BYTES
			.	.	.	.	.	AS
1	0	1	. 1	. 1	. 1	. 1	. 1	REQUIRED
1	. 1	1	. 0	. 0	. 0	. 0	. 0	END BYTE

COMMAND Message: Bit Assignments

- b Odd parity on bytes
- c Even parity on columns
- * Bytes 5, 6, 7, and 8 included if SF16 = 1 & SF8 = 0
- ** Reserved bits

Table 1 Command Message Bit Assignments

A. Reply Message

MSB 8	7	6	5	4	3	2	LSB 1	
b	0	.SC32	.	.	.	.	.SC1	HEADER BYTE
b	0	0	1	DERR	SQ	SX	ERR	BYTE 2
b	0	.SR24	.	.	.	.	.SR19	BYTE 3
b	0	.SR18	.	.	.	.	.SR13	BYTE 4
b	0	SR12	.	.	.	.	.SR7	BYTE 5
b	0	SR6	.	.	.	.	.SR1	BYTE 6
b	1	c	. c	. c	. .	. c	. c	ENDSUM BYTE

b Odd parity on bytes
c Even parity on columns
* Bytes 3, 4, 5, 6 included if SF 16 = 0, SF 8 = 0 (Read)

B. Demand Message

MSB 8	7	6	5	4	3	2	LSB 1	
b	0	SC32	.	.	.	.	.SC1	HEADER BYTE
b	0	1	.SGL5	.	.	.	.SGL1	BYTE 2
b	1	c	c	c	c	c	c	ENDSUM BYTE

b Odd parity on bytes

c Even parity on columns

Table 2 Reply and Demand Message Bit Assignments